Self-analyzing semiconductor IC unit capable of carrying out redundant replacement with installed memory circuits

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Inventor: OSAMU OTANI (JP); TSUKASA OISHI (JP); AL HITAKA HIDETO ET (JP)
Applicant: MITSUBISHI ELECTRIC CORP (JP)
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Built-in self-test circuit and built-in redundancy analysis circuit are provided commonly to plural DRAM cores. Built-in redundancy analysis circuit determines a defective address to be replaced with one of plural spare memory cell rows and plural spare memory cell columns according to an address signal and a detection result of a defective memory cell from built-in self-test circuit. Built-in redundancy analysis circuit controls an effective service area of an address storage circuit into which a defective address is stored according to a capacity of a DRAM core to be tested.